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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS

Appellants:	Jack Linn et al.	**APPEAL BRIEF**
Serial No.	09/846,795	
Filing Date	May 1, 2001	
Group Art Unit	2829	
Examiner	Ashok K. Sarkar	
Attorney Docket No.	125.013US02	
Title: Bonded Substrate for an Integrated Circuit Containing a Planar Intrinsic Gettering Zone		

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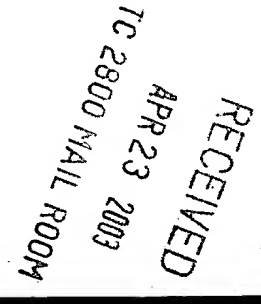
1. Introduction

On February 10, 2003, Appellants filed a notice of appeal from the final rejection of claims 24-44 and 46-48 set forth in the Advisory Action mailed January 22, 2003. Three copies of this Appeal Brief are hereby timely filed on April 15, 2003, and are accompanied by a fee in the amount of $320.00 as required under 37 C.F.R. §1.17(c).



2. Real Party in Interest

The real party in interest in the above-captioned application is the assignee Intersil America Inc.

3. Related Appeals and Interferences

There are no other appeals or interferences known to Appellants that will have a bearing on the Board's decision in the present appeal.

4. Status of the Claims

Claims 24-44 and 46-48 are pending in the application. Claims 49-56 are withdrawn from consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected species. Claims 24-44 and 46-48 are subject of this appeal. In an Advisory Action mailed January 22, 2003 and a Final Office Action mailed June 21, 2002, Claims 24-29, 31, 35-38, 40, 41 and 46-48 were rejected under 35 U.S.C. §102(e) and Claims 30, 32-34, 39 and 42-44 were rejected under 35 U.S.C.§103(a).

5. Summary of the Amendments

No amendments have been made after the Final Office action except for the cancellation of non-elected claims 49-56.

6. Summary of the Invention

In one embodiment, a method of forming semiconductor device is disclosed. The method includes, providing a wafer 22 comprising a monocrystalline semiconductor material. This is illustrated in Figure 2A and is described on page 5, line 15 of the application. Implanting ions 23 of the semiconductor material through a surface of the monocrystalline semiconductor wafer 22 to a selected depth in the wafer 22, thereby forming adjacent to the surface an amorphous layer 25 of the semiconductor material. This is illustrated in Figures 2B and 2C and described on page 5, lines 19-29. The amorphous semiconductor layer 25 extends to a substantially planar zone 27 that is disposed at substantially the selected depth and comprises monocrystalline semiconductor

material damaged by lattice defects. Undamage monocrystalline semiconductor material is located below the selected depth and comprises a second layer 26 of the undamaged monocrystalline semiconductor material. This is illustrated in Figure 2C which is described on page 5 line 30 through page 6, line 4. The wafer 22 is then heated under conditions effective to convert said amorphous semiconductor layer 25 to a first layer 28 of the monocrystalline semiconductor material. This is illustrated in Figure 2D and described on page 6 lines 10 of the application. Further, wafer 22 is heated under conditions effective to coalesce the zone 27 of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone 17 comprising substantially pure semiconductor material and including active gettering sites. The gettering zone 17 is disposed substantially at the selected depth. This is illustrated in Figure 2E and described on Page 6, lines 11-19 of the application. A handle wafer 11 is provided that includes on one surface an insulating bond layer 13. The insulating bond layer 13 is boned to the surface of the wafer 22, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer 11, an insulating bond layer 13, and a monocrystalline semiconductor device wafer. The device wafer contains a substantially planar intrinsic gettering zone 17 that comprises substantially pure semiconductor material and includes active gettering sites. This is illustrated in Figure 3 and is described on page 7, lines 3-27. A semiconductor device is then formed on the second layer 16 (which is also the second layer 26 of the undamaged monocrystalline semiconductor material, please refer to Figures 2D and 2E) undamaged monocrystalline semiconductor material. Alternatively, a layer 18 of epitaxial monocrystalline semiconductor material is deposited on the second layer 16 wherein the semiconductor device is formed on the epitaxial layer 18 (See Figure 4 and the description on page 7, lines 9-8 and lines 27-29.

In another embodiment, a process for forming a semiconductor device is disclosed. The process includes providing a wafer 22 comprising a monocrystalline semiconductor material. This is illustrated in Figure 2A and is described on page 5, line 15 of the application. Implanting ions 23 of the semiconductor material through a surface of the monocrystalline semiconductor wafer 22 to a selected depth in the wafer, thereby forming adjacent to the surface an amorphous layer 25 of the semiconductor material. This is illustrated in Figures 2B and 2C and described on page 5, lines 19-29. The amorphous semiconductor layer 25 extends to a substantially planar zone 27 disposed at substantially the selected depth and comprising monocrystalline

semiconductor material damaged by lattice defects. Undamaged monocrystalline semiconductor material below the selected depth comprise a second layer 27 of the undamaged monocrystalline semiconductor material. Please refer to Figure 2C which is described on page 5 line 30 through page 6, line 4. The wafer 22 is heated under conditions effective to convert the amorphous semiconductor layer 25 to a first layer 28 of the monocrystalline semiconductor material. This is illustrated in Figure 2D and described on page 6 lines 10 of the application. The wafer 22 is further heated under conditions effective to coalesce the zone 27 of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone 17 comprising substantially pure semiconductor material and including active gettering sites. The gettering zone 17 is disposed substantially at the selected depth between the first layer 15 of monocrystalline semiconductor material and the second layer 16 of undamaged monocrystalline semiconductor material. This is illustrated in Figure 2E and described on Page 6, lines 11-19 of the application. A handle wafer 11 is provided that comprises on one surface an insulating bond layer 13. This is illustrated in Figure 3 and described on page 7, lines 3-26. The insulating bond layer 13 is bonded to the surface of the wafer adjacent the first layer 15 of monocrystalline semiconductor material, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer 22 , an insulating bond layer 13, and a monocrystalline semiconductor device wafer 14. This is illustrated in Figure 1 and is described on page 5, lines 6-14. The device wafer 14 contains a substantially planar intrinsic gettering zone 17 that comprises substantially pure semiconductor material and includes active gettering sites, wherein the monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicon ions. The handle wafer comprises silicon and the insulating bond layer comprises silicon dioxide. A semiconductor device is formed on the bonded substrate. This is illustrated in Figure 4 which is described on page 7, line 27 through page 8 line 10 of the application.

In yet another embodiment, a bonded semiconductor-on-insulator substrate for semiconductor devices and integrated circuits is disclosed. The substrate comprises a wafer 22, an insulating bond layer 13 and a handle wafer 11. The wafer 22 comprises mononcrystalline semiconductor material and has a first surface and a second surface. The wafer 22 further comprises a first layer 15 of the monocystalline semiconductor material adjacent to the first surface and a second layer 16 of undamaged monocrystalline semiconductor material adjacent to

the second surface. This is illustrated in Figure 3 and described on page 7, lines 3-26. Moreover, this is also illustrated in Figures 1 and 3 which are described on page 5, lines 6-14 and page 7 line 27 through page 8, line 7 respectfully. Interposed between the first and second layers (15 and 16) of the monocrystalline semiconductor material is a substantially planar intrinsic gettering zone 17 comprising substantially pure semiconductor material and including active gettering sites. The insulating bond layer 13 is disposed on the first surface 15 of said wafer and the handle wafer 11 is bonded to the insulting bond layer 13. This is illustrated in Figure 3 which is described on page 7, lines 3-26. Moreover, this is also illustrated in Figures 1 and 3 which are described on page 5, lines 6-14 and page 7, line 27 through page 8, line 7 respectfully.

In still further another embodiment a bonded semiconductor-on-insulator substrate for an integrated circuit is disclosed. The bonded semiconductor-on-insulator substrate comprises a wafer 22, a handle wafer 11 and an insulating bond layer 13. This is illustrated in Figure 3 and described on page 7, lines 3-26. Moreover, this is also illustrated in Figures 1 and 3 which are described on page 5, lines 6-14 and page 7 line 27 through page 8, line 7 respectfully. The wafer has a first layer 15 of monocrystalline semiconductor material adjacent a first surface of the wafer 22. The wafer 22 further has a second layer 16 of undamaged monocrystalline semiconductor material adjacent a second surface of the wafer 22. The wafer 22 further has a substantially planar intrinsic gettering zone of substantially pure semiconductor material and active gettering sites positioned between the first and second layers formed by implanting ions 23 of the semiconductor material through the first layer of monocrystalline semiconductor material. This is illustrated in Figure 2B which is described on page 5, lines 19-29. The insulating bond layer 13 bonds the handle wafer 11 to the first surface 15 of the wafer 22. This is illustrated in Figure 3 which is described on page 7, lines 3-26.

7. Issues Presented for Review

The questions presented in this Appeal is whether the Examiner erred in rejecting Claims 24-29, 31, 35-38, 40, 41 and 46-48 under 35 U.S.C. §102(b) as being anticipated by US Patent No. 6,083,324 to Henley, claims 30 and 39 under 35 U.S.C.§103(a) as being unpatentable over the Henley reference in view of US Patent No. 5,731,637 to Hori, Claims 32-34 and 42-44 under 35 U.S.C.§103(a) as being unpatentable over the Henley reference.

8. Grouping of Claims

Although, each of claims 24-44 and 46-48 stand or fall on their own merits, Applicant has focused this appeal on the 35 U.S.C. §102(b) rejections of independent Claims 24, 26, 28 and 38 as being anticipated by US Patent 6,083,324 to Henley for brevity reasons. In addition, the rejection of Claims 32-34 and 42-44 under 35 U.S.C. § 103(a) as being unpatentable over Henley et al. and the rejection of Claims 30 and 39 under 35 U.S.C. § 103(a) as being unpatentable over Henley et al. in view of U.S. Patent No. 5,731,637 to Hori are also addressed.

9. Argument

A. Scope and Content of Prior Art

In regards to the 35 U.S.C. §102(b) rejections, the Examiner cited the Henley et al. reference, US Patent No. 6,083,324. The Henley et al. reference relates to a gettering layer formed in silicon-on-insulator wafer. In regards to the 35 U.S.C. § 103(a) rejections, the Examiner cited again cited the Henley et al. reference and the Hori reference, .S. Patent No. 5,731,637. The Hori reference relates to gettering in a high-breakdown-voltage semiconductor device.

B. Rejection of Claims 24, 26, 28 and 38 under 35 U.S.C. §102(b)

i. The Applicable Law

35 U.S.C.§ 102 provides in relevant part:

A person shall be entitled to a patent unless –
(b) the invention was patented or described in a printed publication in this or a foreign country or in a public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A claim is anticipated under 35 U.S.C.§ 102 only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in

the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but identical terminology is not required. *In re Bond*, 910 F. 2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990).

Anticipation focuses on whether a claim reads on a product or process disclosed in a prior art reference, not on what the reference broadly teaches. *Kalman v. Kimberyl-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. v. Guardian Industries Corp.*, 75 F.3d 1558, 37 U.S.P.Q.2d 1618 (Fed. Cir. 1996).

ii. 35 U.S.C. § 102 (b) Rejection Analysis

The Examiner finally rejected independent Claims 24, 26, 28 and 38 under 35 U.S.C. §102(b) as being anticipated by the Henley et al. reference. Specifically, the Examiner asserts that "the product taught by Henley is indistinguishable from the present invention since the heating step in forming Henley's device will heal the implanted damage in Henley's device and restore it to the original undamaged condition as claimed in the instant invention." See the first paragraph, lines 11-13 of the continuation sheet of the Advisory Action, dated January 22, 2003.

Claims 24, 26, 28 and 38 are as follows:

24. A semiconductor device formed by the method comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged monocrystalline semiconductor material below said selected depth comprising a second layer of the undamaged monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a first layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

forming a semiconductor device on said second layer of undamaged monocrystalline semiconductor material or on layer of epitaxial monocrystalline semiconductor material deposited on said second layer; and

wherein the said semiconductor device is formed on said epitaxial layer.

26. A semiconductor device formed by the process comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged monocrystalline semiconductor material below said selected depth comprising a second layer of the undamaged monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a first layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including

active gettering sites, said gettering zone being disposed substantially at said selected depth between the first layer of monocrystalline semiconductor material and the second layer of undamaged monocrystalline semiconductor material;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer adjacent the first layer of monocrystalline semiconductor material, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicon ions;

wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide; and

forming a semiconductor device on said bonded substrate.

28. A bonded semiconductor-on-insulator substrate for semiconductor devices and integrated circuits, said substrate comprising:

a wafer comprising a mononcrystalline semiconductor material and having a first surface and a second surface, said wafer comprising a first layer of the monocystalline semiconductor material adjacent to said first surface and a second layer of undamaged monocrystalline semiconductor material adjacent to said second surface, and interposed between said first and second layers of the monocrystalline semiconductor material, a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites,

an insulating bond layer disposed on said first surface of said wafer;
and

a handle wafer bonded to said insulting bond layer.

38. A bonded semiconductor-on-insulator substrate for an integrated circuit comprising:

a wafer, the wafer having a first layer of monocrystalline semiconductor material adjacent a first surface of the wafer, the wafer further having a second layer of undamaged monocrystalline semiconductor material adjacent a second surface of the wafer, the wafer further having a substantially planar intrinsic gettering zone of substantially pure semiconductor material and active gettering sites positioned between the first and second layers formed by implanting ions of the semiconductor material through the first layer of monocrystalline semiconductor material;

a handle wafer; and

an insulating bond layer bonding the handle wafer to the first surface of the wafer.

Each of the independent Claims 24, 26, 28 and 38 include a similar element of a layer of "undamaged monocrystalline semiconductor material." As illustrated and described in the Application, the undamaged monocrystalline semiconductor material has **not** had ions implanted through it. In particular, referring to Figures 2A-3, the formation of the second layer 16 (undamaged monocrystalline semiconductor layer) is illustrated. Please also refer to the description relating to Figures 2A-3 in the application on page 5, line 15 through page 7, line 27. As illustrated and described, the gettering zone 27 (17) is formed by implanting the ions through the first layer 25 (15) in a wafer 22. Wafer 22 is then inverted (Figure 3) and coupled to the handle wafer 11 so that the damaged monocrystalline semiconductor material (15) is positioned adjacent the handle wafer 11 while the undamaged monocrystalline semiconductor layer 16 (the layer that has not had the ions implanted through it) is positioned away from the handle wafer 11. Devices are then formed on the second undamaged layer 16 or an epitaxial monocrystalline semiconductor layer 18 deposited on the second undamaged layer 16. See Figure 1, Figure 4 and the description on page 7, lines 7-9 and lines 13-15. The objective of the present invention to provide a semiconductor substrate whose electrical characteristics are substantially unchanged by the formation of a gettering zone is achieved with the undamaged monocrystalline

semiconductor layer 16 not having ions implanted through it as is disclosed and claimed in the independent claims 24, 26, 28 and 38.

In contrast, the Henley et al. reference teaches implanting ions through a layer of material. This is illustrated in Figures 1B, 4D and Figures 6B-6E of the Henley et al. reference. Upon this layer that has been implanted through, an epitaxial layer is formed in which active devices are formed. Column 5, lines 32-39 of the Henley et al. reference. The Examiner has argued that a heating step will restore the damage caused by the implantation of ions through the layer converting this layer into undamaged monocrystalline semiconductor material, see page 3 of the Final Office Action dated October 16, 2002 and the continuation sheet of the Advisory Action dated January 22, 2003. However, there is no cleaner (i.e. free of defects) layer of monocrystalline than one that has not been implanted through. The undamaged monocrystalline semiconductor material of the present application (that has **not** been implanted through) achieves the goal of providing a semiconductor substrate whose electrical characteristics are substantially unchanged by the formation of a gettering zone. Accordingly, the Examiner erred in asserting the 35 U.S.C. § 120(b) rejection of the claims because as shown above, not every element as set forth in Claims 24, 26, 28 and 38, are either expressly or inherently taught in the Henley et al. reference. Moreover, the Henley et al reference does not enable one skilled in the art to make the invention as is claimed in Claims 24, 26, 28 and 38 of the present application as is required for a 35 U.S.C. § 120(b) rejection. That is, the Henley et al. reference does not teach the formation of undamaged monocrystalline semiconductor material as is disclosed and claimed in independent claims 24, 26, 28 and 38.

C. Rejection of Claims 32-34, 42-44, 30 and 39 under 35 U.S.C. §103(a)

i. The Applicable Law

35 U.S.C.§ 103 provides in relevant part:

Conditions for patentability; non-obvious subject matter.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was

made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

"The ultimate determination . . . whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: (1) the scope and content of the prior art; (2) the level of ordinary skill in the prior art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness." *In re Dembiczak*, 175 F.3d 994, 998, 50 USPQ2d 1614, 1616 (1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966)).

When applying 35 U.S.C. §103, the claimed invention must be considered as a whole; the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention and a reasonable expectation of success is the standard with which obviousness is determined. *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. MPEP 2143 citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

ii. 35 U.S.C. §103(a) rejection analysis

The Examiner finally rejected Claims 32-43 and 42-44 under 35 U.S.C. §103(a) as being unpatentable over Henley et al. U.S. patent No. 6,083,324. Specifically, the Examiner asserts that:

> Henley fails to expressly teach the thickness of first and second moncrystalline semiconductor layers and the gettering zone.
>
> However, it would have been obvious to one in the art at the time of the invention to judiciously adjust and control these parameters during the formation of the SOI substrate through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and would not yield any unexpected results.

Claims 32-34 and 42-44 of the present application are as follows:

32. The substrate of claim 28 wherein said first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

33. The substrate of claim 28 wherein said second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm.

34. The substrate of claim 28 wherein said gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

42 The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

43. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm.

44. The bonded semiconductor–on-insulator substrate for an integrated circuit of claim 38, wherein the gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

Claims 32-34 and 42-44 should not have been rejected under 35 U.S.C. §103(a) as being unpatentable over Henley. Claims 32-34 and 42-44 address specific dimensions of the various layers that are used to achieve the objectives of the present invention. The Henley reference does not teach or suggest what is claimed in dependant claims 32-34 and 42-45 and their respective independent claims. In particular, the Henley et al. reference does not teach or suggest a first layer on monocyrstalline semiconductor material with a thickness of about 0.1 μm to about 0.8 μm as is disclosed and claimed in Claims 32 and 42 of the present application. Moreover, the Henley reference, alone or in combination, does not teach or suggest a second layer of moncyrstalline semiconductor material with a thickness of about 0.2 μm to about 20 μm as is disclosed and claimed in Claims 33 and 43. In addition, the Henley reference does not teach or suggest a gettering zone with a thickness of about 0.05 μm to about 0.2 μm as is disclosed and claimed in claims 34 and 44 of the present application. Accordingly, a *prima facie* case for obvious has not been shown by the Examiner.

The Examiner further finally rejected claims 30 and 39 under 35 U.S.C. §103(a) as being unpatentable over Henley in view of Hori, US patent No. 5,731,637. Specifically, the Examiner asserted that :

> Henely fails to expressly teach the implantation with Si.
> Hori teaches gettering layers by implanting Si in cloumn3, lines 43-45.
> Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Henley by forming gettering layer with Si implantation since intrinsic gettering layers can be formed by implanting Si taught by Hori.

Claims 30 and 39 are as follows:

30. The substrate of claim 28 wherein the monocrystalline semiconductor material comprises silicon and the substantially planer intrinsic gettering zone is formed by implanting ions of silicon through the first layer of monocrystalline semiconductor material.

39. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the first and second layers of monocrystalline semiconductor comprises silicon and the ions implanted through the first layer are silicon ions.

The Examiner erred in rejecting claims 30 and 39 under 35 U.S.C. §103(a) as being unpatentable over Henley et al. in view of Hori. Neither the Henley et al. nor Hori reference alone or in combination teach or suggest all the elements found in Claims 30 or 39 and their respective independent claims of the present application. In particular, neither the Henley et al. nor Hori reference alone or in combination teach or suggest "implanting ions of silicon through the first layer of monocrystalline semiconductor material," or "ions implanted through the first layer are silicon ions," as is disclosed and claimed in respective Claims 30 and 39. In particular neither one of the references teach or suggest implanting silicon ions through the "first layer" as the "first layer" is disclosed and claimed in the present application. Since, the teaching or suggesting requirement of each limitation for a 103 rejection has not been met, a *prima facie* case for obvious has not been shown by the Examiner.

10. Summary

Appellants have set forth reasons why the Examiner is incorrect in maintaining his rejections of the pending claims. Specifically, the Examiner has failed to set forth a prima facie case of anticipation or obviousness. The Henley et al. reference nor the Hori reference teach all the limitations in the pending independent and dependant claims. Appellant respectfully submits that, for the above reasons, Claims 24-44 and 46-48 are allowable over the cited art, either alone or in combination. Therefore, reversal of the Examiner's rejections are respectfully requested.

Respectfully submitted,

Date: 4-15-03

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Appendix 1

Claims on Appeal

24. A semiconductor device formed by the method comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged

monocrystalline semiconductor material below said selected depth comprising a second layer of the undamaged monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a first layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

forming a semiconductor device on said second layer of undamaged monocrystalline semiconductor material or on layer of epitaxial monocrystalline semiconductor material deposited on said second layer; and

wherein the said semiconductor device is formed on said epitaxial layer.

25. The semiconductor device of claim 24 wherein said device is selected form the group consisting of a bipolar junction transistor, a field effect transistor, a capacitor, a resistor, a thyristor and combinations thereof comprising integrated circuits.

26. A semiconductor device formed by the process comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged monocrystalline semiconductor material below said selected depth comprising a second layer of the undamaged monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a first layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth between the first layer of monocrystalline semiconductor material and the second layer of undamaged monocrystalline semiconductor material;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer adjacent the first layer of monocrystalline semiconductor material, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline

semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicon ions;

wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide; and

forming a semiconductor device on said bonded substrate.

27. The semiconductor device of claim 26 wherein said device is selected from the group consisting of a bipolar junction transistor, a field effect transistor, a capacitor, a resister, a thyristor, and combinations thereof comprising integrated circuits.

28. A bonded semiconductor-on-insulator substrate for semiconductor devices and integrated circuits, said substrate comprising:

a wafer comprising a mononcrystalline semiconductor material and having a first surface and a second surface, said wafer comprising a first layer of the monocystalline semiconductor material adjacent to said first surface and a second layer of undamaged monocrystalline semiconductor material adjacent to said second surface, and interposed between said first and second layers of the monocrystalline semiconductor material, a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites,

an insulating bond layer disposed on said first surface of said wafer;
and

a handle wafer bonded to said insulting bond layer.

29. The substrate of claim 28 wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicon ions.

30. The substrate of claim 28 wherein the monocrystalline semiconductor material comprises silicon and the substantially planer intrinsic gettering zone is formed by implanting ions of silicon through the first layer of monocrystalline semiconductor material.

31. The substrate of claim 28 wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide.

32. The substrate of claim 28 wherein said first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

33. The substrate of claim 28 wherein said second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm.

34. The substrate of claim 28 wherein said gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

35. The substrate of claim 28 further comprising two or more devices and one or more trenches surrounding at least one of said devices for laterally isolating the surrounded device form the other device(s).

36. A semiconductor device formed on the second layer of monocrystalline semiconductor material of the substrate of claim 28 or on a layer of epitaxial monocrystalline semiconductor material deposited on said second layer.

37. The semiconductor device of claim 36 wherein said device is selected form the group consisting of a bipolar junction transistor, field effect transistor, capacitor, a resistor, a thyristor, and combinations thereof comprising integrated circuits.

38. A bonded semiconductor-on-insulator substrate for an integrated circuit comprising:

a wafer, the wafer having a first layer of monocrystalline semiconductor material adjacent a first surface of the wafer, the wafer further having a second layer of undamaged monocrystalline semiconductor material adjacent a second surface of the wafer, the wafer further having a substantially planar intrinsic gettering zone of substantially pure semiconductor material and active gettering sites positioned between the first and second layers formed by implanting ions of the semiconductor material through the first layer of monocrystalline semiconductor material;

a handle wafer; and

an insulating bond layer bonding the handle wafer to the first surface of the wafer.

39. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the first and second layers of monocrystalline semiconductor comprises silicon and the ions implanted through the first layer are silicon ions.

40. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the second layer of undamaged monocrystalline semiconductor material is a device layer upon which semiconductor devices are formed.

41. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the handle wafer comprises silicon and the insulating bond layer comprises silicon dioxide.

42 The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

43. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm.

44. The bonded semiconductor–on-insulator substrate for an integrated circuit of claim 38, wherein the gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

45. Canceled

46. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, further comprising:

a layer of epitaxial monocrystalline semiconductor material deposited on the second layer.

47. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 46, further comprising:

two or more semiconductor devices formed in the epitaxial monocrystalline semiconductor material, wherein the semiconductor devices are laterally isolated form each other.

48. The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, further comprising:

two or more semiconductor devices formed in the bonded semiconductor-on-insulator substrate, wherein each semiconductor device is laterally isolated from each other.

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Title: BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANAR INTRINSIC GETTERING ZONE

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Enclosures

The following documents are enclosed:
X An Appeal Brief (in triplicate, original plus two copies) (23 pgs.).
X Credit Card Payment Form (1 pg.), for filing a brief in support of an appeal under 37 C.F.R. 1.17(c).
X An itemized return receipt postcard.

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I certify that this correspondence, and the documents identified above, are being deposited with the United States Postal Service as first class mail in an envelope addressed to: BOX AF, Commissioner for Patents, Washington, D.C. 20231 on April 15, 2003.

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